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Multi-Hole Process Plate Modification for Chip on Lead Device at Die Attach Process

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Authors' contributions

This work was carried out in collaboration amongst the authors. All authors read, reviewed, and approved the final manuscript.

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ABSTRACT

The paper focused on the improvement done in chip on lead (COL) leadframe package assembly manufacturing to address the leadframe bouncing effect during die attach process. A new and enhanced process plate is designed with multi-hole configuration to provide a strong vacuum underneath the leadframe and to maintain the planarity during dispensing and die bonding of silicon dies onto the leadframe. With the new multi-hole process plate, leadframe bouncing was successfully eliminated during die attach process. For future works, the multi-hole process plate could be used on devices with similar configuration.

Keywords: Chip on lead; die attach; leadframe bouncing; process plate; vacuum hole.

1. INTRODUCTION

Chip on lead (COL) leadframe package is one of the highest volume runners in semiconductor assembly manufacturing industry, and this COL package need to maintain its competitive market position and its value as well. New technologies have a given manufacturability issues encountered during lot processing and one of the process mostly affected is die attach process. This COL package comes up with a material of conductive and non-conductive adhesives underneath the silicon dies and the leadframe has an extended lead and serves as die attach or

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die bonding area during the attaching of silicon dies at die attach process. Die attach process is responsible in attaching of silicon dies from a wafer tape to a leadframe or substrate carrier. Note that with new and continuous technology trends, development, and state-of-the-art platforms come along challenges in assembly manufacturing [1-4].

The paper focused on the solution and improvement done to mitigate the bouncing effect on the carrier by modifying the process plate from single hole to a multi-hole. A process plate is an assembly tooling used in die attach process to serve as base support platform of the leadframe or carrier. It has vacuum holes to suck or pull the leadframe or carrier in order to have a stable dispensing and die bonding during the attaching of silicon dies. If the interface between the leadframe and the process plate is not stable, a gap could occur as shown in Fig. 1, which may lead to leadframe bouncing during the die attach process.

2. PROBLEM IDENTIFICATION

A complete assembly process flow for chip on lead device in attention from pre-assembly to singulation is illustrated in Fig. 2. Highlighted with red line is the process mostly affected with the concern issue of leadframe bouncing. Important to note that assembly manufacturing process flow differs with the technology and hence the product [5-7]. As earlier mentioned, with continuing technology development and breakthroughs, challenges in assembly manufacturing are unavoidable.

Leadframe bouncing during attaching of silicon dies is the top major assembly reject during die attach process, and this was seen during the lot processing of the device. This leadframe bouncing is caused by a single-hole process plate that the vacuum hole cannot totally suck the leadframe or the carrier. Illustrated in Fig. 3a. Is the single-hole process plate and Fig. 3b is the cross-sectional view of the process plate and leadframe during die attach process. The vacuum hole is located underneath the leadframe pad or carrier wherein the diameter and the design of the hole can be modified.

It is important that leadframe bouncing be eliminated as it will result to further assembly issues such crumpled strips, leadframe bending and dents, warpage, uneven bonding of die, localized insufficient epoxy, and misaligned die encountered during the conversion and setup stage of die attach process. Assembly issues on succeeding processes could also occur due to the leadframe bouncing effect such as non-stick on pad or non-stick on lead during wirebonding process and mold epoxy bleed or mold flash at molding process.

3. METHODS AND RESULTS

With the new and enhanced process plate design as shown in Fig. 4, improved stability of during die attach process was achieved. No more gaps were seen between the interface of the process plate and the leadframe.

The relocation of vacuum pad from the middle of the carrier to sideways design improved the bonding stability of silicon die. The improved process plate design would avoid potential damage to the backside of the carrier resulted from unbalanced bonding and vacuum hole diameter. With this new design of process using the multi-hole, the silicon die would now stick properly on the die paddle due to elimination of the bouncing effect during bonding. Bond line thickness of the package would eventually improve as well as the package reliability. Furthermore, increasing the number of vacuum holes creates better and improved control for the leadframe carrier during the process. After completing the 10 line stressing lots using the multi-hole process plate, leadframe bouncing has been successfully eliminated as depicted in Fig. 4. Note that the actual parts per million (ppm) level are purposely not shown due to confidentiality.

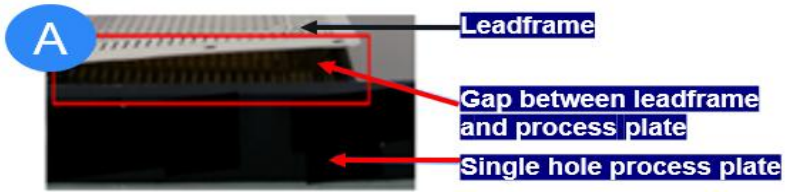

Fig. 1. Gap between the leadframe and the process plate

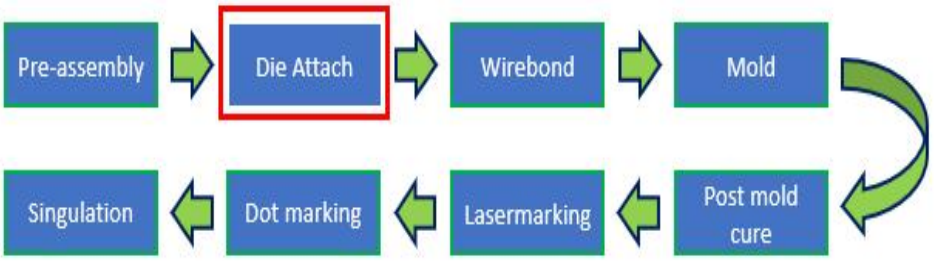

Fig. 2. Chip on lead assembly process flow

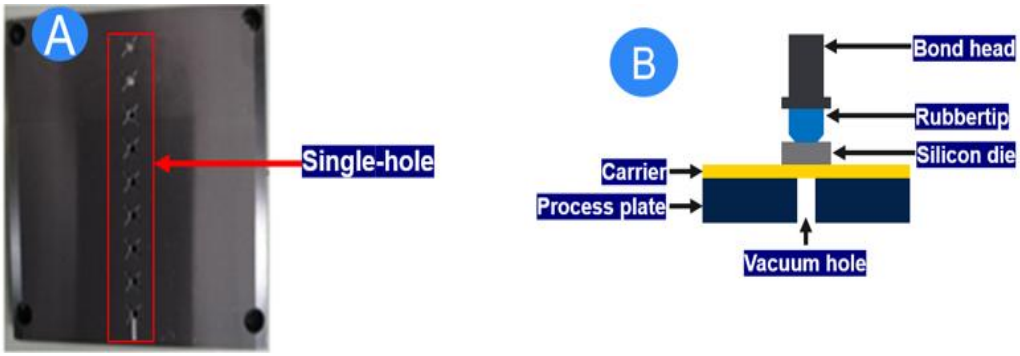

Fig. 3. a) Single-hole process plate; b) cross-sectional view of the process plate and leadframe during die attach process

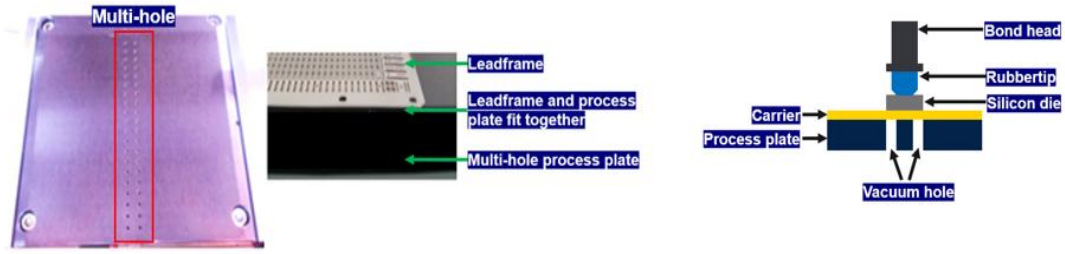

Fig. 4. Multi-hole process plate design, showing the vacuumed semiconductor leadframe carrier

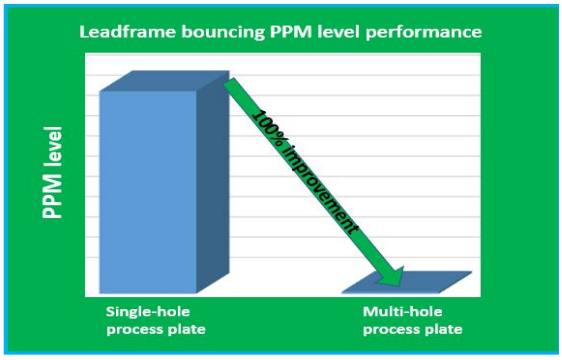

Fig. 5. PPM level performance of leadframe bouncing

4. CONCLUSION

The paper discussed a process solution and improvement done with the enhanced process plate that significantly improved the issue encountered at die attach process which is the leadframe bouncing during the attaching of silicon dies. The improved process plate provided stable die bonding of silicon dies, better bond line thickness response, and eventual good reliability tests. For succeeding works, the multi-hole process plate could be used on packages with similar requirement.

Although the paper focused on the improvement in the process plate to address the die attach process related defects, continuous process and design improvement is important to sustain high quality performance of semiconductor chip on lead packages and its assembly manufacturing. Studies and learnings discussed in [3,8-11] are helpful in improving the assembly manufacturing processes particularly the die attach process.

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COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Tsukada Y, et al. Trend of semiconductor packaging, high density and low cost. Proceedings of the 4th international symposium on electronic materials and packaging, Taiwan. 2002;1-6.
2. Saha S. Emerging business trends in the semiconductor industry. Proceedings of PICMET '13: Technology management in the IT-Driven services (PICMET) USA. 2013;2744-2748.
3. Xian TS, Nanthakumar P. Dicing die attach challenges at multi die stack packages. 35th IEEE/CPMT International Electronics Manufacturing Technology conference, Malaysia. 2012;1-5.
4. Yeap LL. Meeting the assembly challenges in new semiconductor packaging trend. 34th IEEE/CPMT International Electronic Manufacturing Technology Symposium (IEMT), Malaysia. 2010;1-5.
5. Nenni D, McLellan P. Fabless: The transformation of the semiconductor industry. CreateSpace Independent Publishing Platform, USA; April 2014.
6. Doering R, Nishi Y. Handbook of semiconductor manufacturing technology. 2nd ed., CRC Press, USA; July 2007.
7. Geng H. Semiconductor manufacturing handbook. 2nd ed., McGraw-Hill Education, USA; September 2017.
8. Graycochea Jr. E, et al. Warpage mitigation through diebond process improvement with enhanced leadframe configuration. Journal of Engineering Research and Reports. 2020;10(2);39-42.
9. Abdullah Z, et al. Die attach capability on ultra thin wafer thickness for power semiconductor. 35th IEEE/CPMT International Electronics Manufacturing Technology Conference, Malaysia: 2012;1-5.
10. Sumagpang Jr A, et al. Non-stick on pad defect reduction through clamp and insert design augmentation. Journal of Engineering Research and Reports. 2020;12(2);37-45.
11. Abdullah S, et al. Dicing die attach film for 3D stacked die QFN package. 32nd IEEE/CPMT International Electronic Manufacturing Technology Symposium. USA. 2007;73-75.

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